DATA SHEET

SCN68562

Dual universal serial communications controller (DUSCC)

Product specification

1995 May 01

IC19 Data Handbook

Philips
Semiconductors

PHILIPS

Dual universal serial communications controller (DUSCC) SCN68562

DESCRIPTION

The Philips Semiconductors SCN68562 Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented and character-oriented (byte count and byte control) synchronous data link controls as well as asynchronous protocols. The SCN68562 interfaces to the 68000 MPUs via asynchronous bus control signals and is capable of program-polled, interrupt driven, block-move or DMA data transfers. The operating mode and data format of each channel can be programmed independently.

Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a digital phase-locked loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common bit rate generator (BRG), operating directly from a crystal or an external clock, which provides 16 common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits per second are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

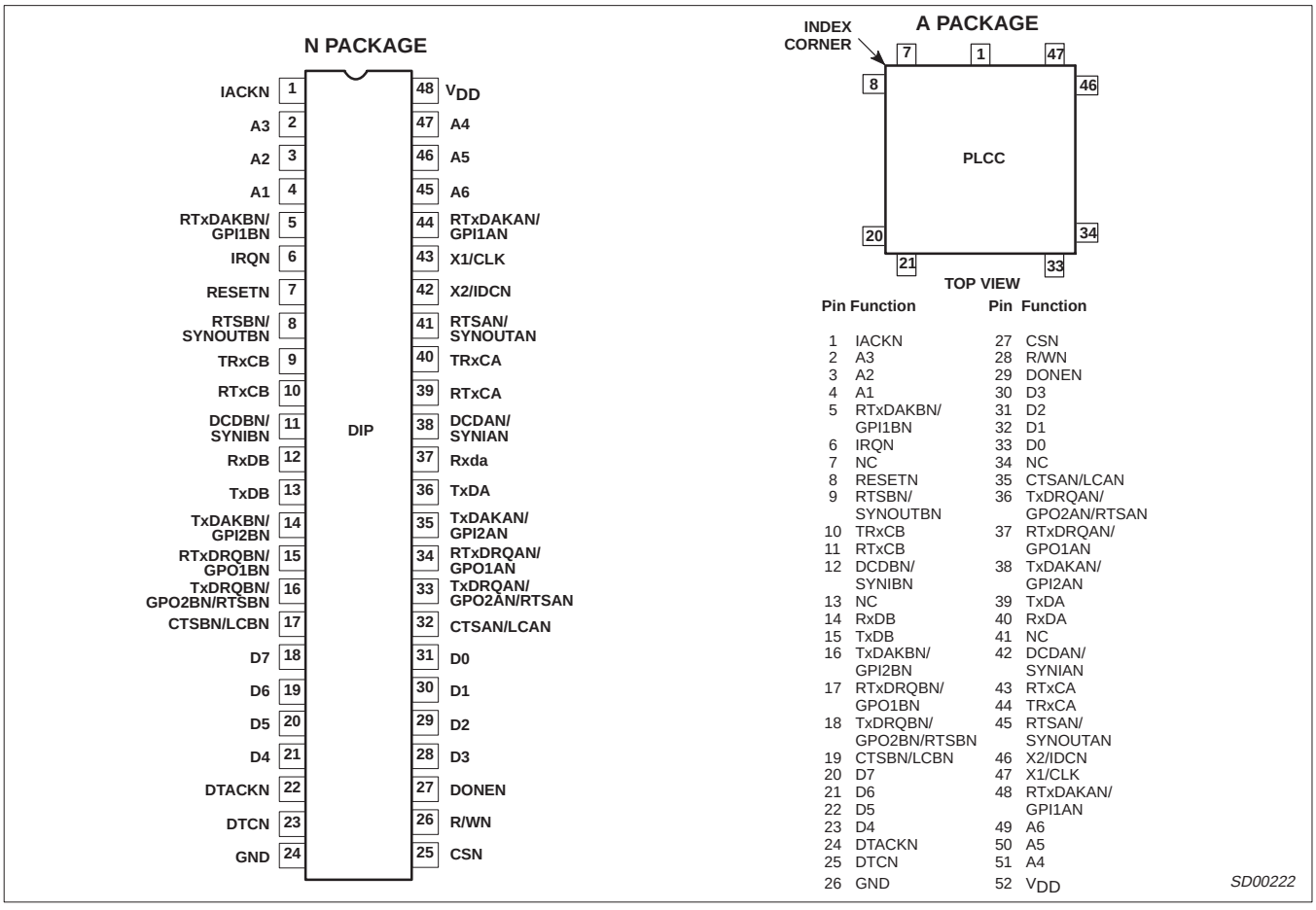
Two modem control inputs (DCD and CTS) and three modem control outputs are provided. These inputs and outputs can be optionally programmed for other functions.

FEATURES

General Features

- Dual full-duplex synchronous/asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5–8 bits plus optional parity
- Four character receiver and transmitter FIFOs

PIN CONFIGURATIONS



Pin	Function	Pin	Function
1	IACKN	27	CSN
2	A3	28	R/WN
3	A2	29	DONEN
4	A1	30	D3
5	RTxDAKBN/ GPI1BN	31	D2
		32	D1
6	IRQN	33	D0
7	NC	34	NC
8	RESETN	35	CTSAN/LCAN
9	RTSBN/ SYNOUTBN	36	TxDRQAN/ GPO2AN/RTSAN
10	TRxCB	37	RTxDRQAN/ GPO1AN
11	RTxCB		
12	DCDBN/ SYNIBN	38	TxDAKAN/ GPI2AN
13	NC	39	TxDA
14	RxDB	40	RxDA
15	TxDB	41	NC
16	TxDAKBN/ GPI2BN	42	DCDAN/ SYNIAN
17	RTxDRQBN/ GPO1BN	43	RTxCA
		44	TRxCA
18	TxDRQBN/ GPO2BN/RTSBN	45	RTSAN/ SYNOUTAN
19	CTSBN/LCBN	46	X2/IDCN
20	D7	47	X1/CLK
21	D6	48	RTxDAKAN/ GPI1AN
22	D5		
23	D4	49	A6
24	DTACKN	50	A5
25	DTCN	51	A4
26	GND	52	V_{DD}

Figure 1. Pin Configurations

- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (frame check sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM0, FM1, Manchester
- Programmable channel mode: full- and half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Compatible with the Philips Semiconductors SCB68430 Direct Memory Access Interface (DMAI) and other DMA controllers
  - Single- or dual-address dual transfers
  - Half- or full-duplex operation
  - Automatic frame termination on counter/timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
- Multi-function programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2-bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmits up to 4Mbs and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK line-fill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection

BISYNC Features

- EBCDIC or ASCII header, text and control messages
- SYN, DLE stripping
- EOM (end of message) detection and transmission
- Auto transparent mode switching
- Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
- Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0–7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS FLAGs line-fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

ORDERING INFORMATION

DESCRIPTION	V_{CC} = +5V ±5%, T_A = 0°C to +70°C Serial Data Rate = 4Mbps Maximum	DWG #
48-Pin Plastic Dual In-Line Package (DIP)	SCN68562C4N48	SOT240-1
52-Pin Plastic Leaded Chip Carrier (PLCC) Package	SCN68562C4A52	SOT238-3

NOTE: See SCN26562/SCN68562 User's Guide for detailed description of all the features.

BLOCK DIAGRAM

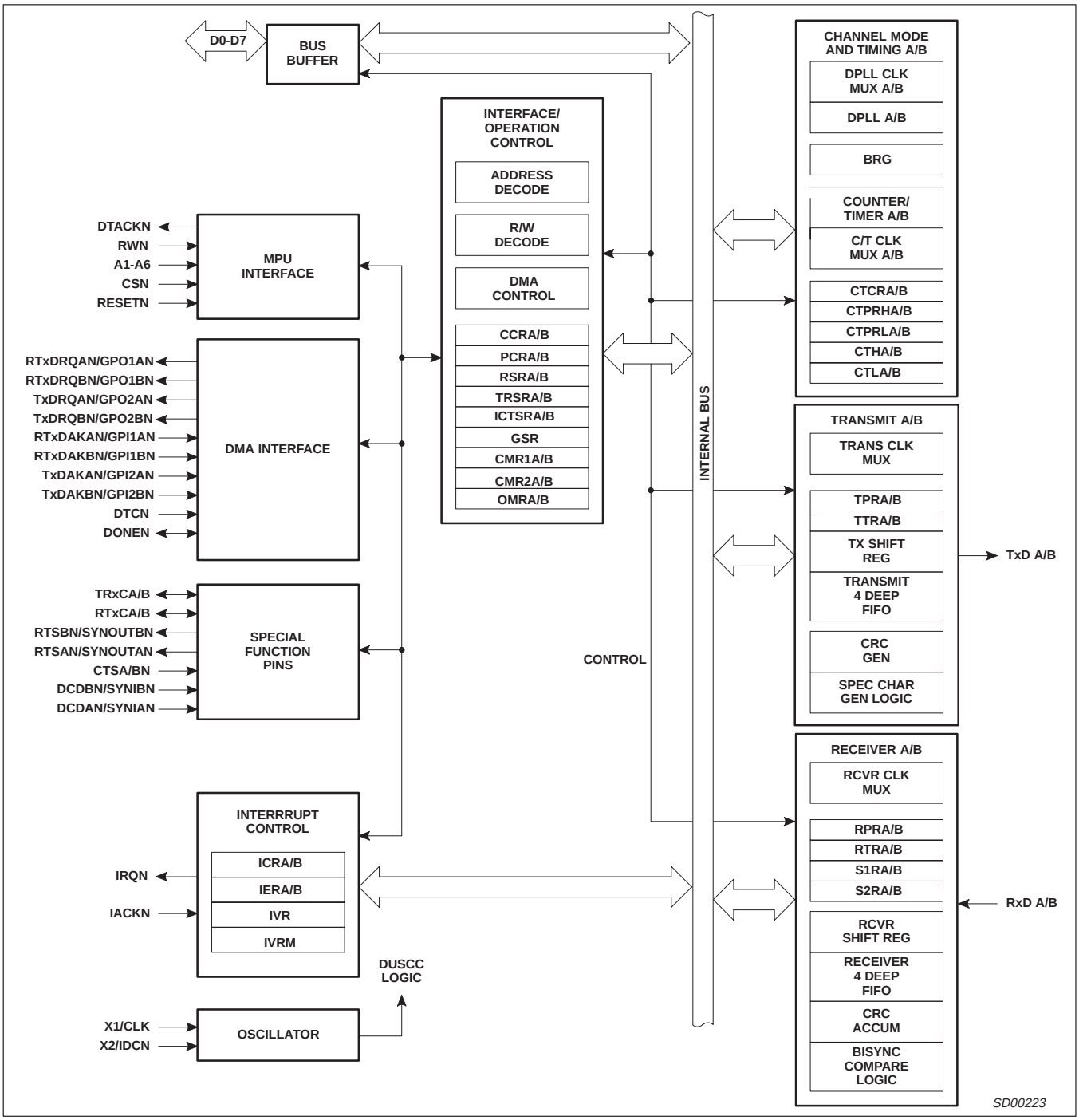


Figure 2. Block Diagram

PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 – A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 – D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 – D7 as controlled by the R/WN and A1 – A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 – D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1 of the CDUSCC Users' Guide. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to-Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V $\pm$ 10% power input.
GND	24	I	Signal and power ground input.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_{CC}	Voltage from V_{CC} to GND[3]	-0.5 to +7.0	V
V_S	Voltage from any pin to ground[3]	-0.5 to V_{CC} +0.5	V

NOTES:
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 40°C/W for plastic DIP and 42°C/W for PLCC.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.

DC ELECTRICAL CHARACTERISTICS[1, 4]

T_A = 0 to +70°C, V_{CC} = 5.0V ± 5%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage:					
	All except X1/CLK				0.8	V
	X1/CLK				0.4	V
V_{IH}	Input high voltage:					
	All except X1/CLK		2.0			V
	X1/CLK		2.4		V_{CC}	V
V_{OL}	Output low voltage:					
	All except IRQN, DONEN	I_{OL} = 5.3mA			0.5	V
	IRQN, DONEN	I_{OL} = 8.8mA			0.5	V
V_{OH}	Output high voltage:					
	(Except open drain outputs)	I_{OH} = -400µA	2.4			V
I_{ILX1}	X1/CLK input low current[3]	V_{IN} = 0, X2 = GND	-5.5		0.0	mA
I_{IHX1}	X1/CLK input high current[3]	V_{IN} = V_{CC}, X2 = GND			1.0	mA
I_{ILX2}	X2 input low current[3]	V_{IN} = 0, X1 = open	-100			µA
I_{IHX2}	X2 input high current[3]	V_{IN} = V_{CC}, X1 = open			100	µA
I_{IL}	Input low current DTCN, TxDAKA/BN, RTxDAKA/BN	V_{IN} = 0	-40			µA
I_L	Input leakage current	V_{IN} = 0 to V_{CC}	-5		5	µA
I_{OZH}	Output off current high, 3-State data bus	V_{IN} = V_{CC}			5	µA
I_{OZL}	Output off current low, 3-State data bus	V_{IN} = 0	-5			µA
I^{ODL}	Open drain output low current in off	V_{IN} = 0				
	state: DONEN		-120		-25	µA
	IRQN, DTACKN		-5			µA
I_{ODH}	Open drain output high current in off	V_{IN} = V_{CC}				
	state: DONEN, IRQN, DTACKN				5	µA
I_{CC}	Power supply current	V_O = 0 to V_{CC}			275	mA
C_{IN}	Input capacitance[2]	V_{CC} = GND = 0			10	pF
C_{OUT}	Output capacitance[2]	V_{CC} = GND = 0			15	pF
$C_{I/O}$	Input/output capacitance[2]	V_{CC} = GND = 0			20	pF

NOTES:
1. Parameters are valid over specified temperature and voltage range.
2. These values were not explicitly tested; they are guaranteed by design and characterization data.
3. X1/CLK and X2 are not tested with a crystal installed.
4. This specification applies to revision D, revision E and later revisions.

AC ELECTRICAL CHARACTERISTICS[1, 2, 3, 4] T_A = -55 to +110°c, V_{CC} = 5V ± 10%

NO.	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
1	3	RESETN pulse width	1.2			µS
2	4,6	A1 - A6 set-up time to CSN Low	10			nS
3	4,6	A1 - A6 hold time from CSN High	0			nS
4	4,6	RWN set-up time to CSN Low	0			nS
5	4,6	RWN hold time to CSN High	0			nS
6	4,6	CSN High pulse width[4]	160			nS
7	4,5	CSN or IACKN High from DTACKN Low	30			nS
7A	5	IACKN High to DTACKN High			200	nS
8	4,5	Data valid from CSN or IACKN Low			300	nS
9	4	Data bus floating from CSN High[7]			100	nS
10	6	Data hold time from DTACKN Low[5]	0			nS
11	4,6	DTACKN Low from read data ready	0			nS
12	4,6	DTACKN Low from CSN Low			560	nS
12A	6	CSN Low to write data valid			50	nS
13	4,6	DTACKN High from CSN High			150	nS
14	4,6	DTACKN high impedance from CSN High			185	nS
15	5	DTACKN Low from IACKN Low			550	nS
16	8	GPI input set-up time to CSN Low	20			nS
17	8	GPI input hold time from CSN Low	100			nS
18	8	GPO output valid from DTACKN Low			300	nS
19	9	IRQN High from:				
		Read RxFIFO (RxRDY interrupt)			450	nS
		Write TxFIFO (TxRDY interrupt)[8]			450	nS
		Write RSR (Rx condition interrupt)[8]			400	nS
		Write TRSR (Rx/Tx interrupt)[8]			400	nS
		Write ICTSR (port change and CT int.)[8]			400	nS
20	10	X1/CLK High or Low time	25			nS
		X1/CLK frequency	2.0	14.7456	16	MHz
		CTCLK High or Low time	100			nS
		CTCLK frequency	0		4	MHz
		RxC High or Low time	110			nS
		RxC frequency (16X or 1X)[9]	0		4	MHz
		TxC High or Low time	110			nS
		TxC frequency (16X or 1X)	0		4	MHz
21	11	TxD output from TxC input Low (1X)			240	nS
		(16X)			435	nS
22	11	TxD output from TxC output Low			50	nS
23	12	RxD data set-up time to RxC High	50			nS
24	12	RxD data hold time from RxC High	50			nS
25	13	IACKN Low to daisy chain Low			200	nS
26	15	Data valid from receive DMA ACKN			300	nS
27	14,15	DTCN width	100			nS
28	14,15	RDYN Low to DTCN Low	80			nS
29	15	Data bus float from DTCN Low[7]			200	nS
30	14,15	DMA ACKN Low to RDYN (DTACKN) Low			360	nS
31	14,15	RDYN High from DTCN Low			230	nS
32	14,15	RDYN High impedance from DTCN Low			250	nS
33	15	Receive DMA REQN High from DMA ACKN Low			325	nS
34	15	Receive DMA ACKN width	150			nS
35	14,15	Receive DMA ACKN Low to DONEN Low			250	nS
36	14	Data set-up to DTCN Low	50			nS
37	14	Data hold from DTCN Low[6]	50			nS
38	14	Transmit DMA REQN High from ACKN Low			340	nS
39	14	Transmit DMA ACKN width	150			nS
40	14	Transmit DMA ACKN Low to DONEN Low output			250	nS
40A	14	DTCN Low DONEN output High			260	nS
41	16	CSN Low to transmit DONEN Low output			300	nS

NO.	FIGURE	PARAMETER	LIMITS			UNIT
			Min	Typ	Max	
42	16	CSN Low to transmit DMA REQ negated			400	nS
43	16	CSN Low to receive DONEN Low			300	nS
44	16	CSN Low to receive DMA REQ negated			400	nS

NOTES:
1. Parameters are valid over specified temperature range.
2. All voltage measurements are referenced to ground (GND). For DC and functional testing, all inputs except X1/CLK swing between 0.8V and 2.0V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 2.4V All time measurements are referenced at input voltages of 0.4V and 2.4V for all inputs. Output levels are referenced at 1.2V and 2.0V, as appropriate.
3. Test conditions for outputs: C_L = 150pF, except open-drain outputs. Test condition for open-drain outputs: C_L = 50pF to GND, R_L = 2.7kΩ to V_{CC} except DTACKN whose R_L = 820Ω to V_{CC} and C_L = 150pF to GND and DONEN which requires C_L = 50pF to GND and R_L = 1kΩ to V_{CC}.
4. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
5. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
6. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
7. These values were not explicitly tested, they are guaranteed by design and characterization data.
8. These timings are from the falling edge of DTACKN (not CSN rising).
9. X1/CLK frequency must be at least four times the receiver serial data rate.

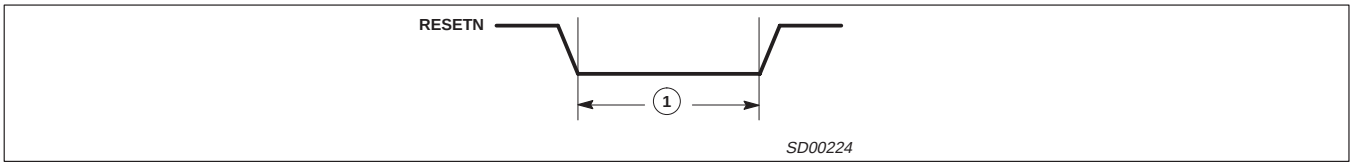


Figure 3. Reset Timing

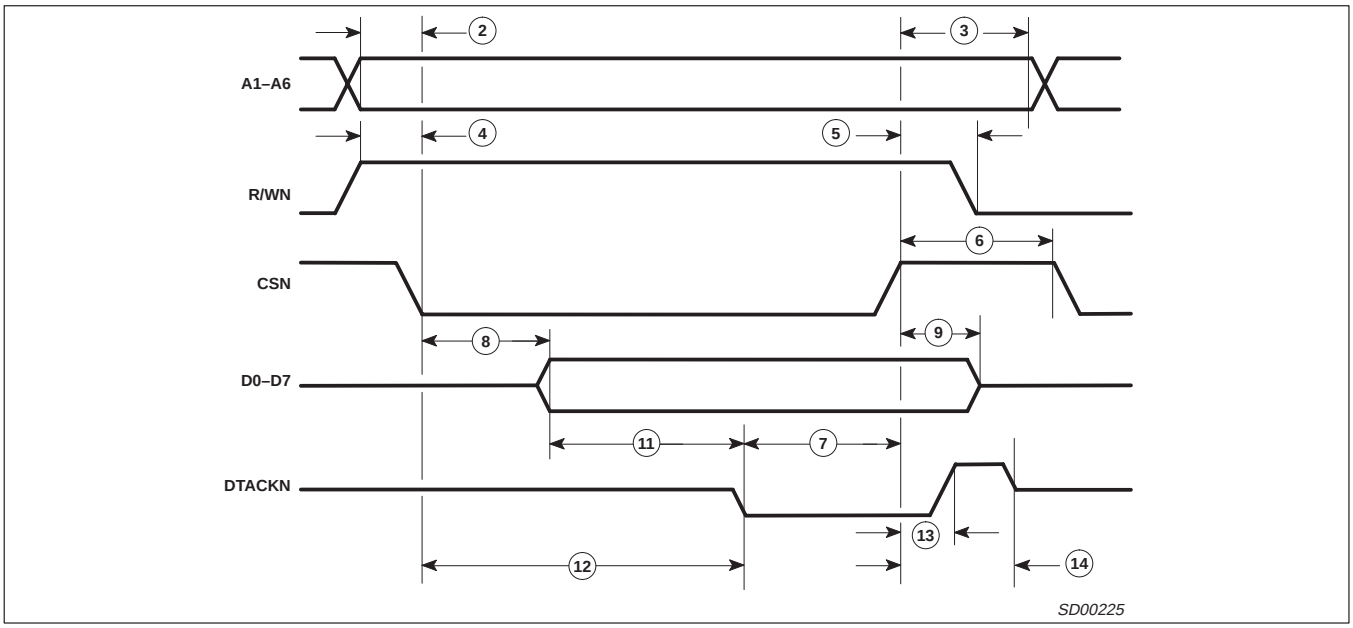


Figure 4. Bus Timing (Read Cycle)

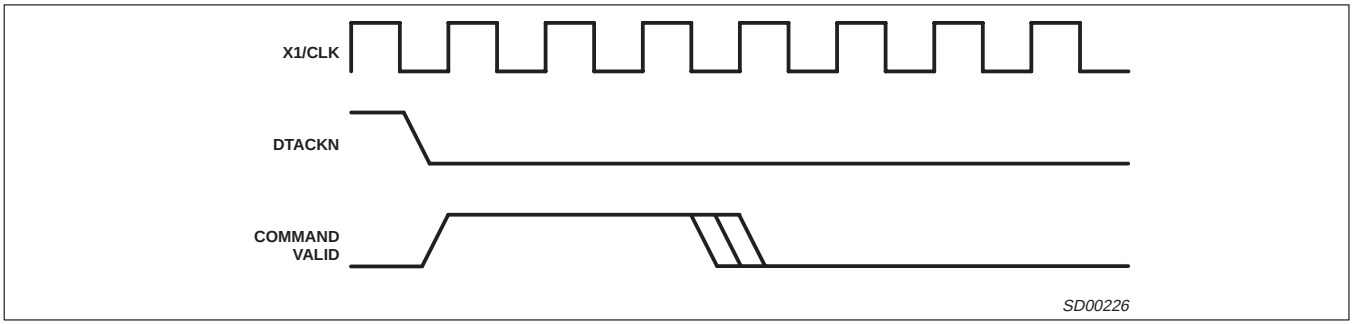


Figure 5. Command Timing

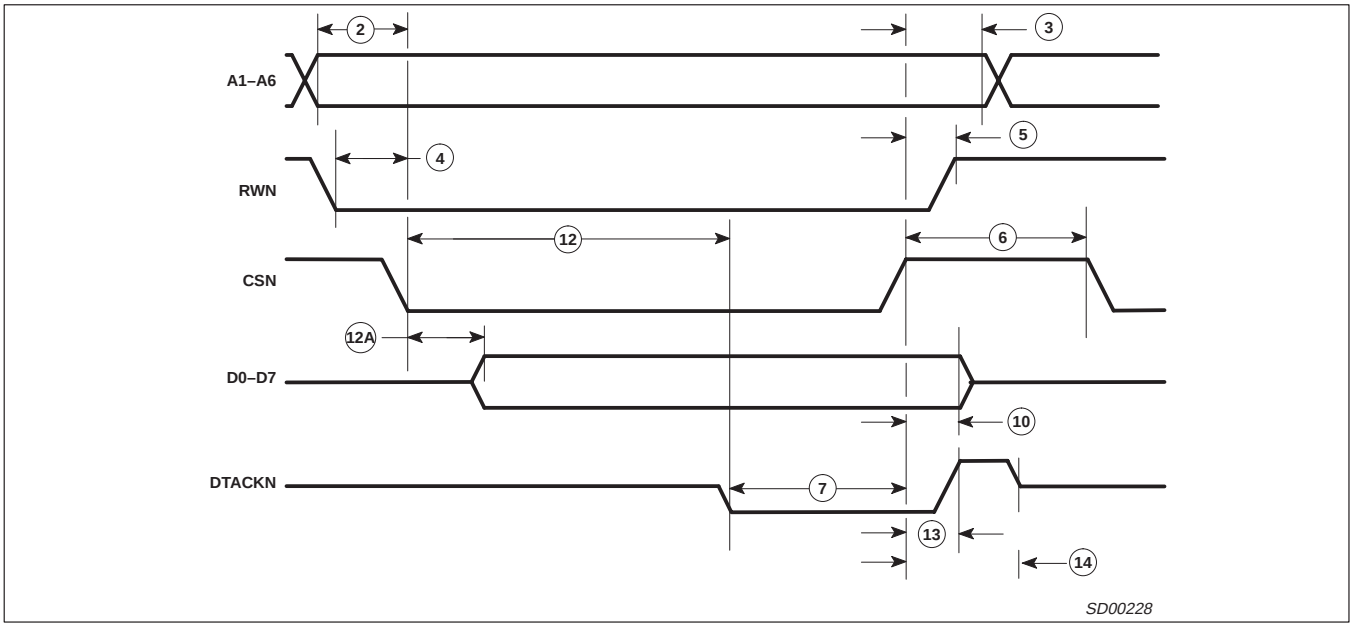


Figure 6. Bus Timing (Write Cycle)

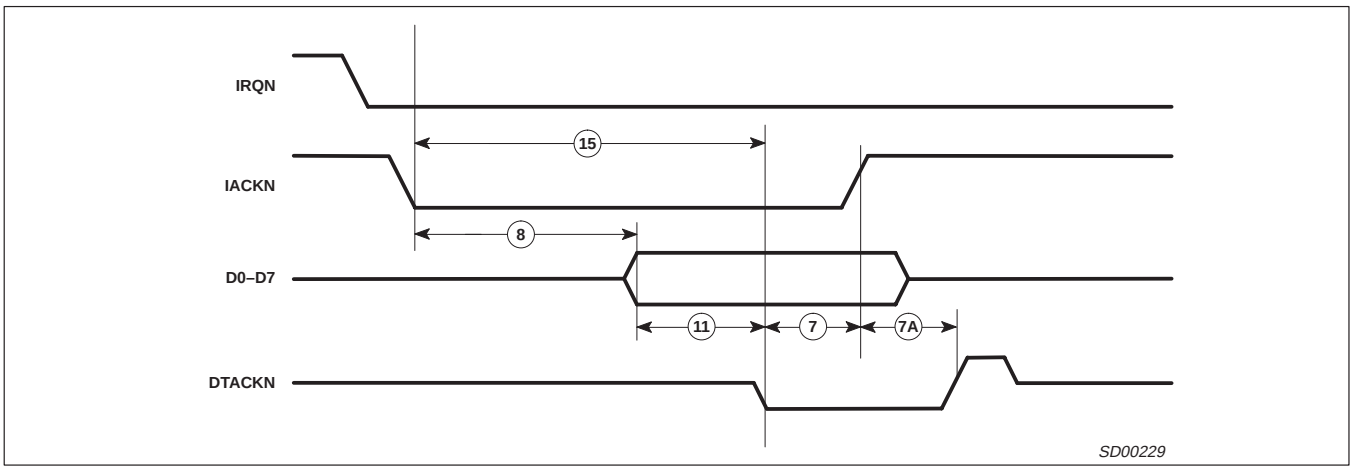


Figure 7. Interrupt Cycle Timing

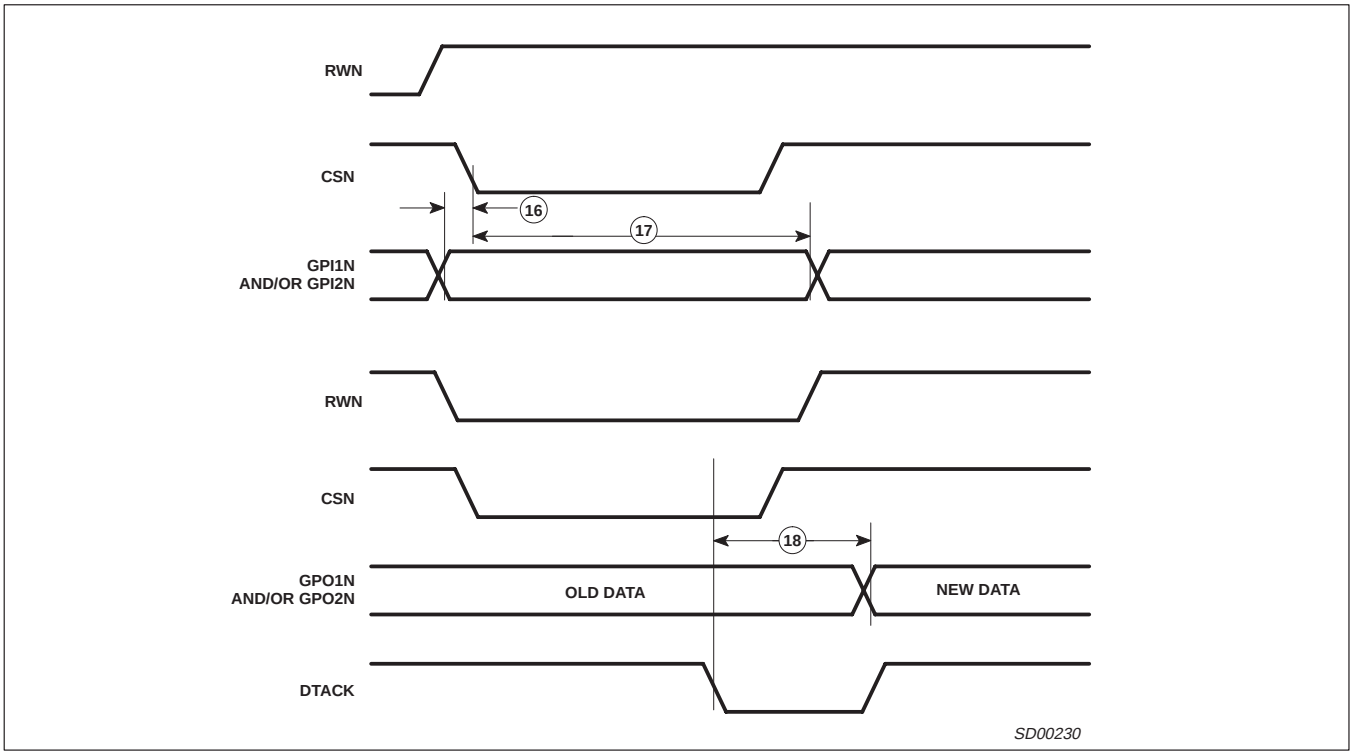


Figure 8. Port Timing

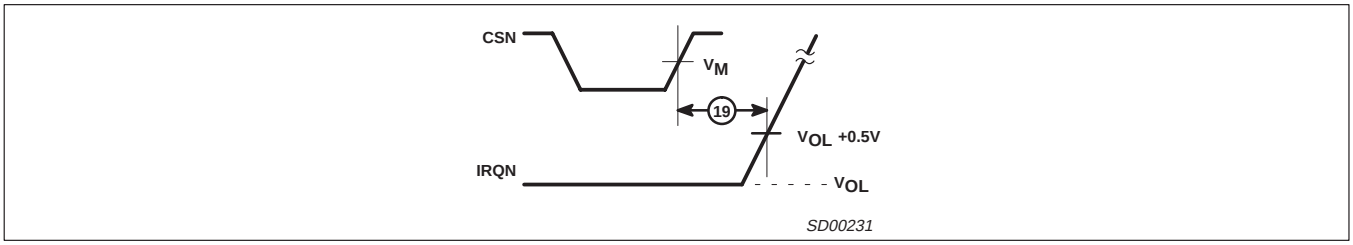


Figure 9. Interrupt Timing

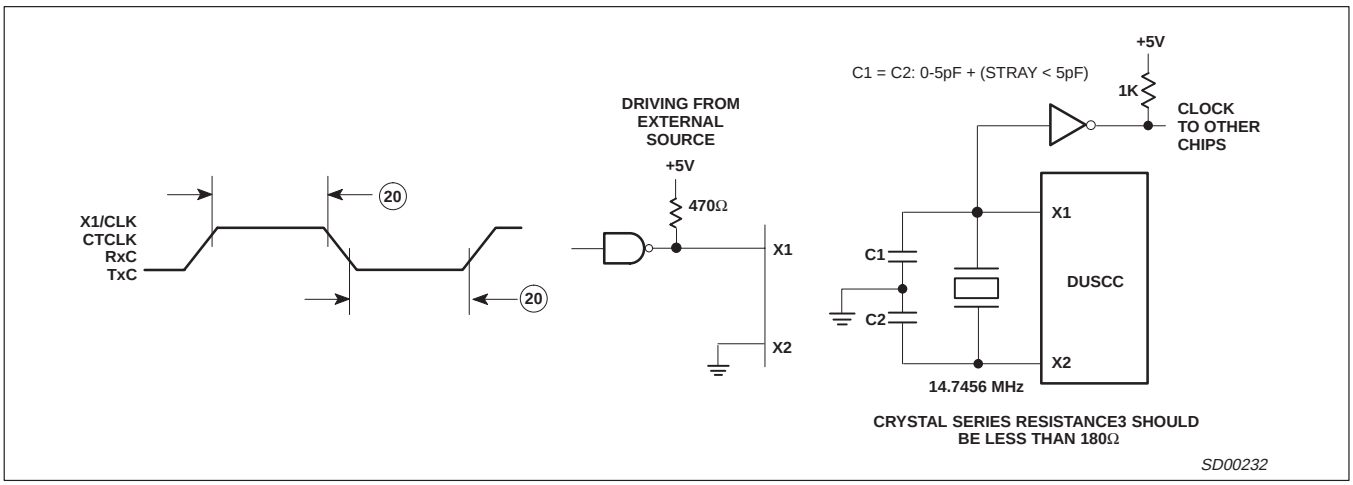


Figure 10. Clock Timing

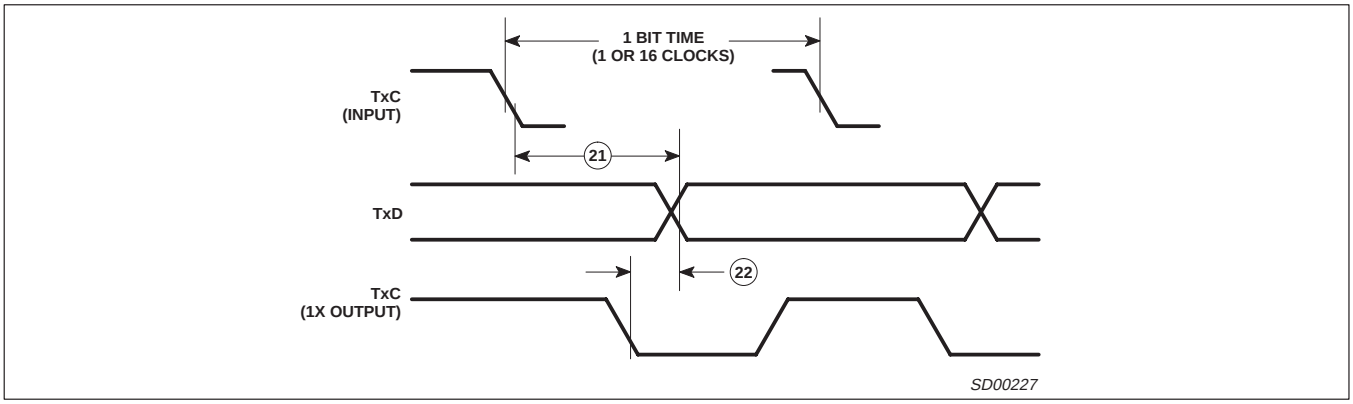


Figure 11. Transmit Timing

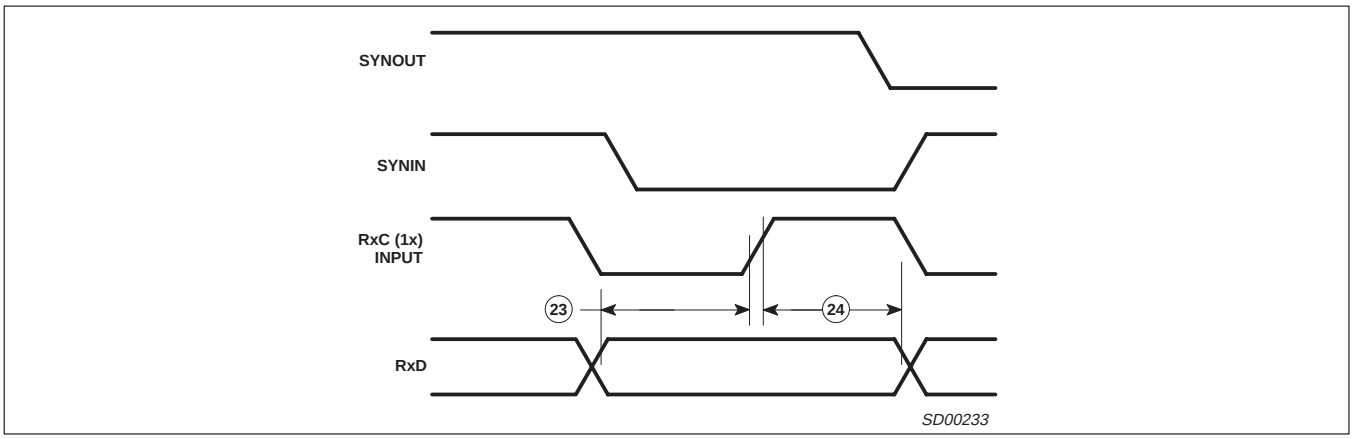


Figure 12. Receive Timing

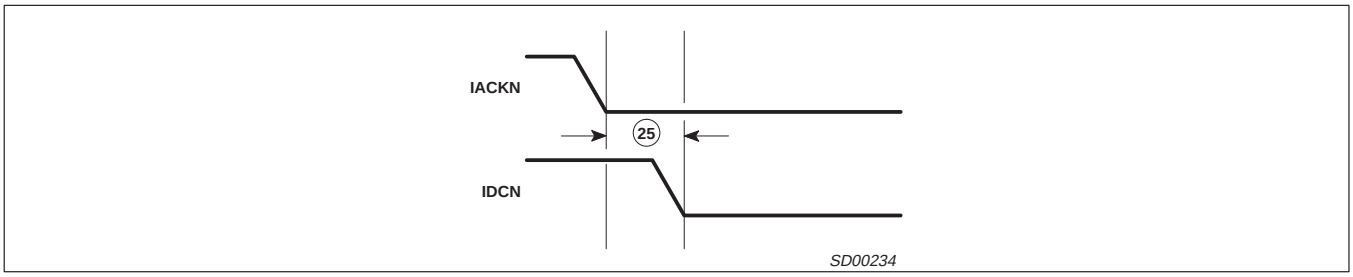


Figure 13. Interrupt Daisy Chain Timing

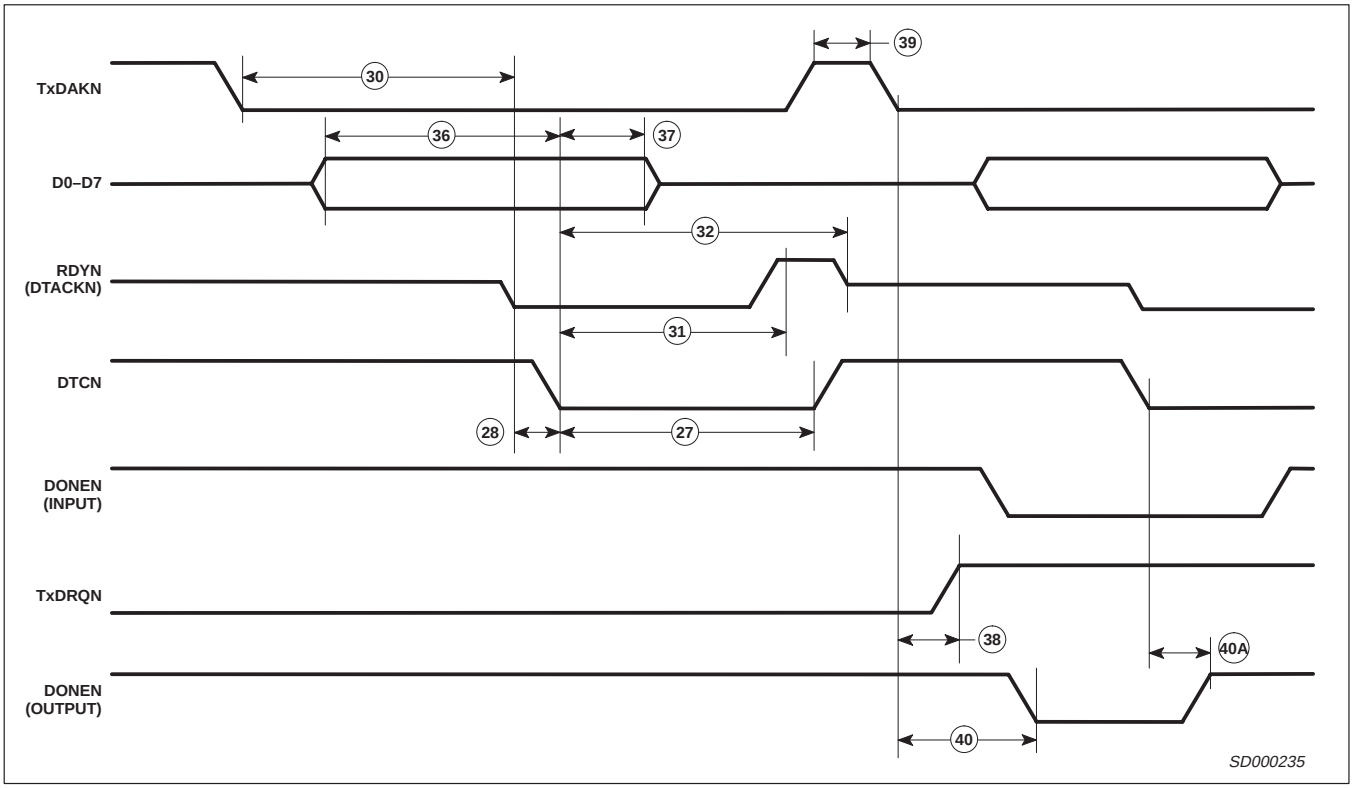


Figure 14. DMA Transmit Write Timing—Single Address DMA Mode

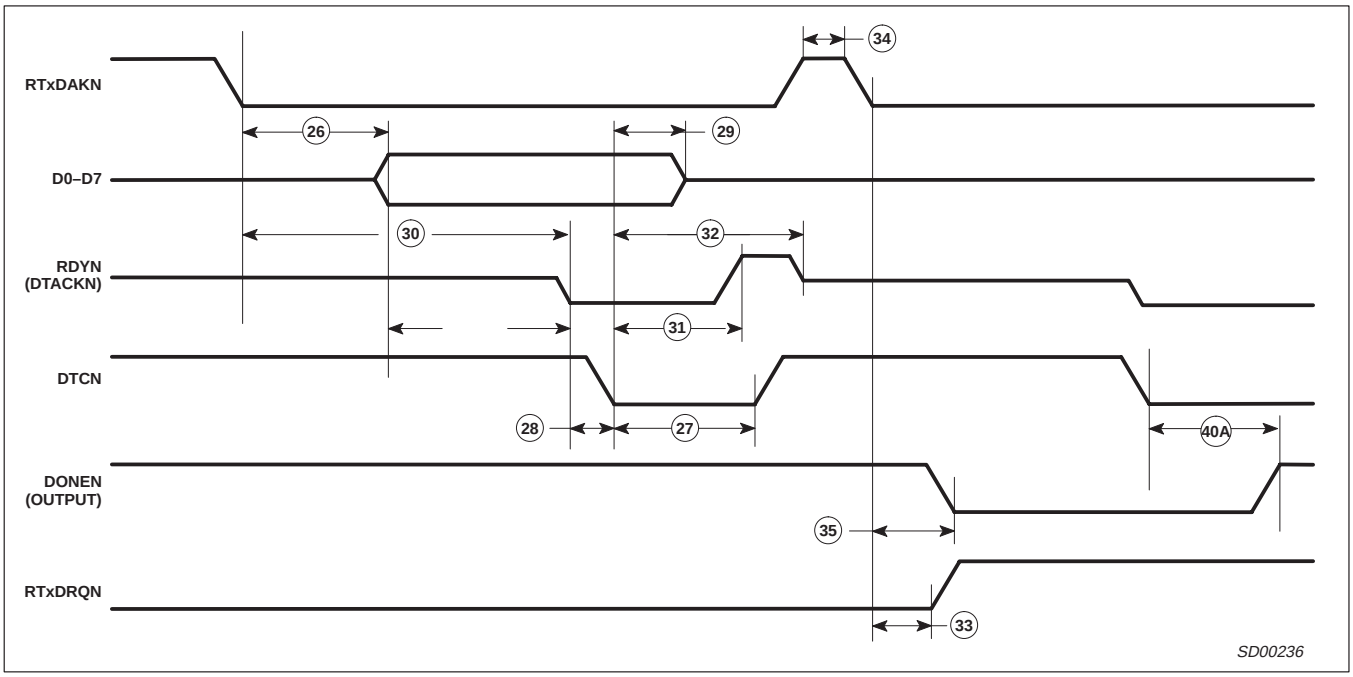


Figure 15. DMA Receive Read Timing—Single Address DMA Mode

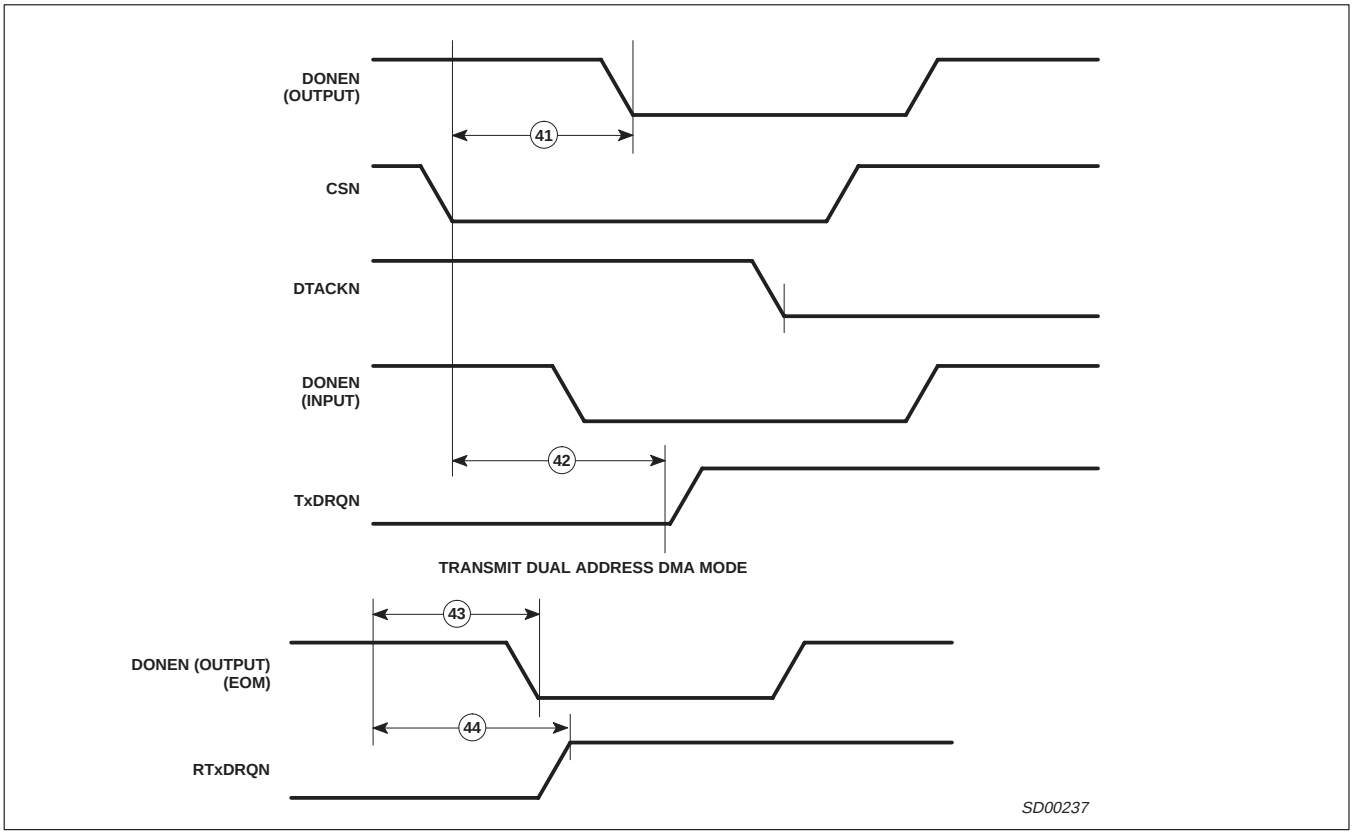
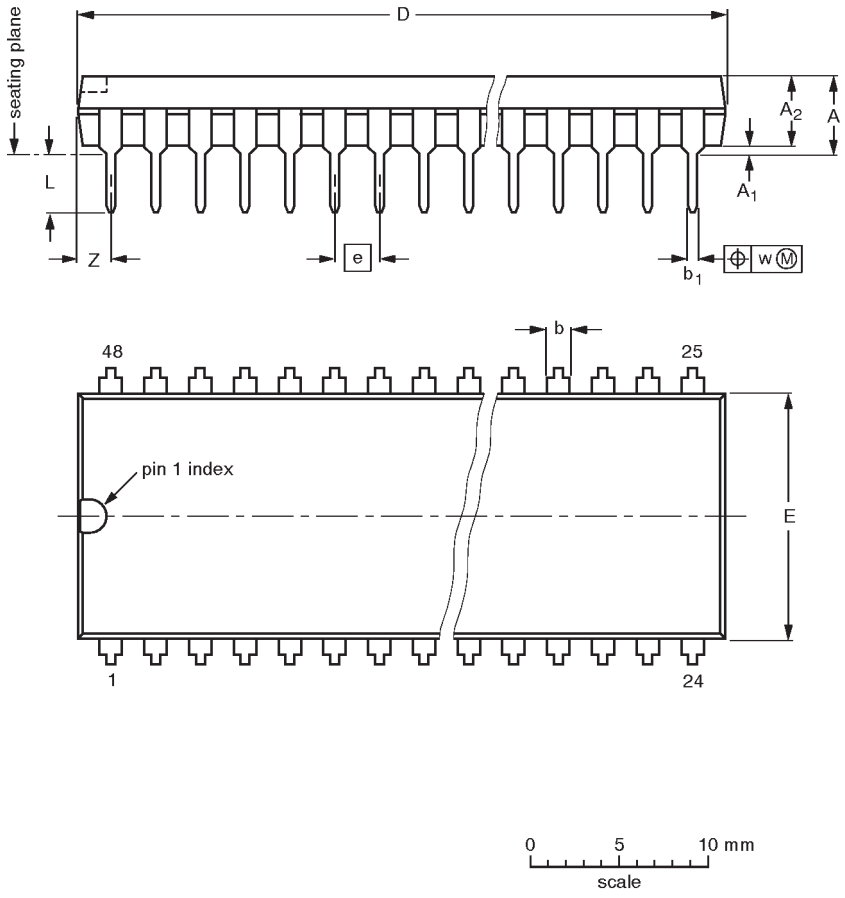


Figure 16. Dual Address DMA Mode Timing

DIP48: plastic dual in-line package; 48 leads (600 mil) **SOT240-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

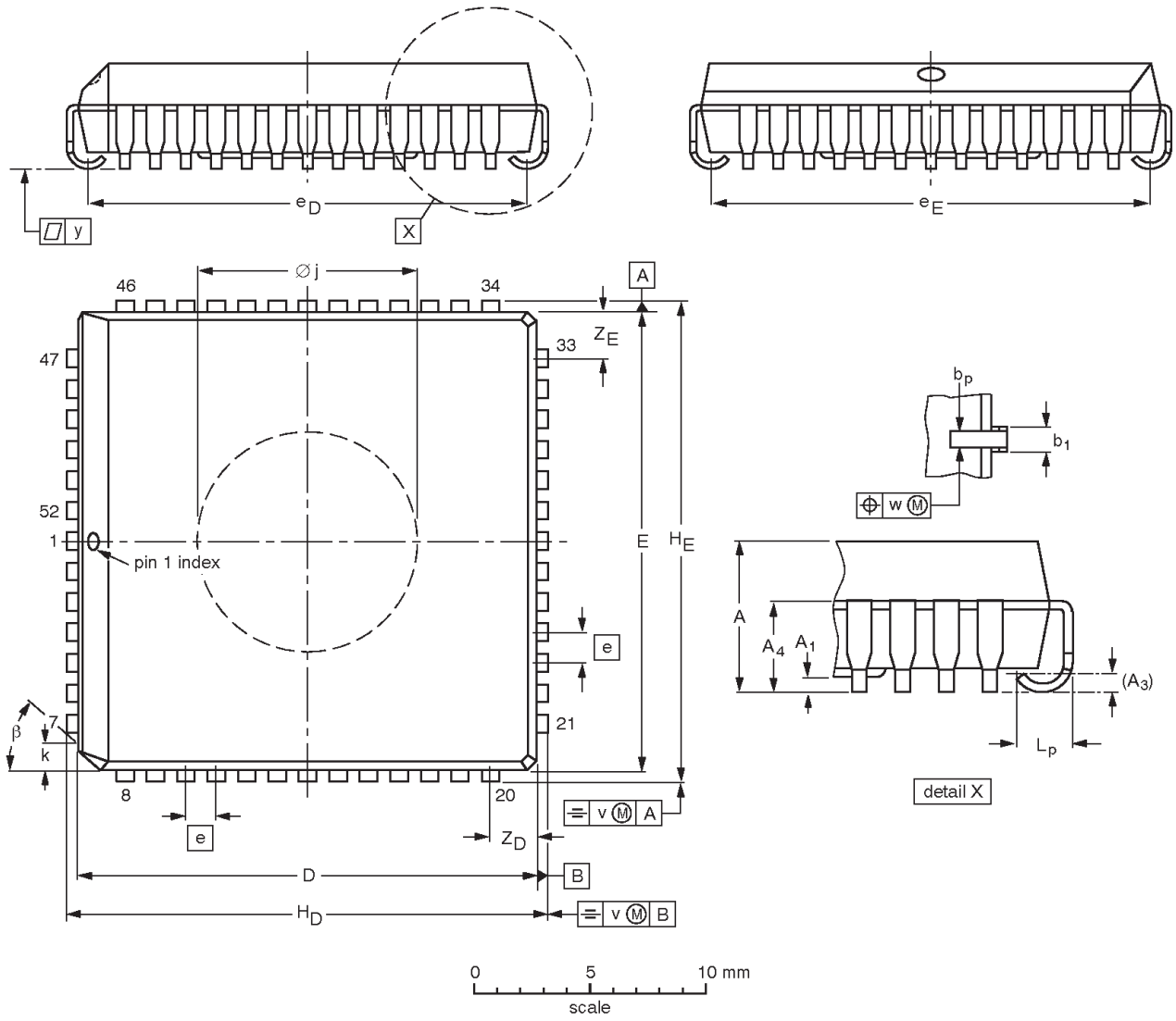
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.9	0.36	4.06	1.4 1.14	0.53 0.38	0.36 0.23	62.60 61.60	14.22 13.56	2.54	15.24	3.90 3.05	15.88 15.24	18.46 15.24	0.254	2.1
inches	0.19	0.014	0.16	0.055 0.045	0.021 0.015	0.014 0.009	2.46 2.42	0.56 0.53	0.10	0.60	0.15 0.12	0.63 0.60	0.73 0.60	0.01	0.083

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT240-1						~~92-11-17~~ 95-01-25

PLCC52: plastic leaded chip carrier; 52 leads; pedestal **SOT238-3**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$\varnothing_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	19.20 19.05	19.20 19.05	1.27	18.54 17.53	18.54 17.53	20.19 19.94	20.19 19.94	1.22 1.07	9.25 9.09	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.756 0.750	0.756 0.750	0.05	0.730 0.690	0.730 0.690	0.795 0.785	0.795 0.785	0.048 0.042	0.364 0.358	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT238-3		MO-047AD				~~95-02-25~~ 97-12-16

NOTES

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Data sheet status	Product status	Definition [1]
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